ECR #: 28
Title: Control Setup and Output Valid Time
Release Date: Mar. 3, 1997
Impact: Change
Spec Version: A.G.P. 1.0

Summary: Separate the timings of the control and data paths and take 0.5 ns from the tVALID time of control lines and add 0.5 ns to the setup time tSU for data and 1.0 ns to the setup time for control signals. Also, reduce tPROP to 2.5 ns.

Background: Data inputs are not used to make bus state transition decisions in AGP, whereas control inputs are. Control inputs have considerably more logic in their input paths and this logic must make decisions for the next clock cycle. This is requiring more setup time for control inputs than for data lines. However, because control signals do not have as much loading on their output enable paths their output delays (tVALID) can be reduced a bit. This reduction can be added to the setup time for control paths. This change gains about 0.5 ns of setup time. Another 0.5 ns is needed and can come from the reduced tPROP.

Reducing tVALID (max.) makes it harder to hit tVALID (min.), so it is also proposed that tVALID (min.) be set at 1.0 ns and the data hold times be returned to 0 ns.

Also, recent motherboard simulations of data-strobe skew due to crosstalk show that to meet the 700 ps tRMATCH values, the flight times (tPROP) need to be less than 2.5 ns. This will be discussed in a future release of the A.G.P. Design Guide.

Note: During the investigations into the viability of this proposal, a further observation was made. The clock skew between two A.G.P. compliant components (tSKEW) acts to reduce the time available to propagate control signals or data signals in A.G.P.-1X mode exactly in the manner of tPROP. In fact, the system requirement is that the clock skew be less than 1.0 ns to account for hold times and that the sum of tPROP and tSKEW be less than 3.5 ns to account for setup times. This is not proposed as a spec change, but will be noted in a future version of the A.G.P. Design Guide.

Change Current Specification as shown:

1. Separate A.G.P.-1X Control and Data timing specs:

For Control Signals (REQ#, GNT#, FRAME#, IRDY#, TRDY#, SERR#, ST[2::0], PIPE#, RBF#, DEVSEL#):
tSU = 6.0(min.) tDH = 0.0(min.) tVALID(max.) = 5.5 tVALID(min.) = 1.0

For Data Signals (AD[31::0], CBE[3::0]#):
tSU = 5.5(min.) tDH = 0.0(min.) tVALID(max.) = 6.0 tVALID(min) = 1.0

Note: The strobe signals are not affected by these specs as they are only used in A.G.P.-2X mode.

2. Reduce tPROP

tPROP = 2.5 ns (max.)

Specific Change Text Attached Below

Table 00-11: A.G.P. 1X AC Timing Parameters

Symbol	Parameter	Min	Max	Units	Notes
…					
Transmitter Output Signals:					
t_{VALC}	CLK to control signal valid delay	1.0	5.5	ns	4
t_{VALD}	CLK to data valid delay	1.0	6.0	ns	4
t_{ON}	Float to Active Delay	1.0	6	ns	
t_{OFF}	Active to Float Delay	1	14	ns	
Receiver Input Signals:					
t_{SUC}	Control signals setup time to CLK	6.0		ns	4
t_{SUD}	Data setup time to CLK	5.5		ns	4
t_{H}	Control signals hold time to CLK	0.0		ns	4
…					

The following changes are based on the changes already in place from ECR-12

Table 4-8: Interconnect Delay Summary

Symbol	Parameter	Max[1]	Units	Notes
t_{PROP}	Signal propagation	**2.5**	ns	2
$t_{PROP-MB}$	Signal propagation, motherboard	**1.65**	ns	5,9
$t_{PROP-CONN}$	Signal propagation, connector	**.15**	ns	9
$t_{PROP--CARD}$	Signal propagation, add-in card	**.7**	ns	6,9
$t_{TRMATCH}$	Total Trace mismatch between Data and Strobe	**.7**	ns	3,4,7,8, 9
$t_{TRMATCH-MB}$	Trace mismatch, motherboard	**.5**	ns	4,7,9
$t_{TRMATCH-CARD}$	Trace mismatch, card	**.2**	ns	4,8,9

NOTES:
1. Signal propagation delays are measured as the difference between the driver driving a 10pf lumped load vs. the driver driving an 80ohm transmission line terminated by a 10pf lumped load.
2. Tprop is the sum of all other propagation delays
3. Ttrmatch is the sum of all trace mismatches.
4. Trace mismatch applies between signal groups and their associated strobes: **AD_STB1=>AD[31::16]** & **C/BE[3::2]#**; **AD_STB0=>AD[15::0]** & **C/BE[1::0]#**; **SB_STB=>SBA[7::0]**. The trace mismatch spec only applies between the strobe and data signals within a group, not between data signal within a group or between groups.
5. Recommended Baseboard trace lengths: 1.0 - 9 (inches) depending on trace spacing.
6. Recommended Add-in card trace lengths: 0.0 - 3.0 (inches).
7. Recommended Baseboard matching between any Data trace and its associated **STB#** trace:
   L_data - L_stb = -0.5 to 0.0 (inches).
8. Recommended Add-in card matching between any Data trace and its associated **STB#** trace:
   L_data - L_stb = -0.5 to +0.5 (inches).
9. Trace length and trace length matching are recommendations based on interconnect simulations including a wide variety of transmission line and loading effects. Designers must ensure through simulation or other techniques that the interconnect timing requirements will still be met.

Table 4-10: Motherboard Interconnect Delays

Symbol	Parameter	Max[1]	Units	Notes
$t_{PROP-MB}$	Signal propagation, motherboard	**1.65**	ns	3,5
$t_{PROP-CONN}$	Signal propagation, connector	**.15**	ns	5
$t_{TRMATCH-MB}$	Trace mismatch, motherboard	**.5**	ns	2,4,5

Notes:
1. Signal propagation delays are measured as the difference between the driver driving a 10pf lumped load vs. the driver driving an 80ohm transmission line terminated by a 10pf lumped load.
2. Trace mismatch applies between signal groups and their associated strobes: **AD_STB1=>AD[31::16]** & **C/BE[3::2]#**; **AD_STB0=>AD[15::0]** & **C/BE[1::0]#**; **SB_STB=>SBA[7::0]**. The trace mismatch spec only applies between the strobe and data signals within a group, not between data signal within a group or between groups.
3. Recommended Baseboard trace lengths: 1.0 - 9 (inches) depending on trace spacing.
4. Recommended Baseboard matching between any Data trace and its associated **STB#** trace:
   L_data - L_stb = -0.5 to 0.0 (inches).
5. Trace length and trace length matching are recommendations based on interconnect simulations including a wide variety of transmission line and loading effects. Designers must ensure through simulation or other techniques that the interconnect timing requirements will still be met.